Sub CS

20. (Amended) A method of partitioning a shared memory, comprising:

setting a configuration register to partition said shared memory into a first plurality of memory banks and a second plurality of memory banks;

accessing said first plurality of memory banks from a first agent;

accessing said second plurality of memory banks from a second agent; and

re-partitioning said shared memory on-the-fly;

wherein said second agent receives a clock signal representation of said first agent's clock signal.

REMARKS

Claims 1, 7 and 20 are amended herein. Claims 1-8 and 10-23 remain pending in the application.

Claims 13 and 16 over Satoh

In the Office Action, claims 13 and 16 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Satoh et al., U.S. Patent No. 5,999,197 ("Satoh"). The Applicants respectfully traverse the rejection.

Claims 13 and 16 recite, *inter alia*, a first agent providing a memory access clock signal and a second agent providing **a representation of the memory access clock signal** to access a shared memory **in synchronism with access by the first agent** to the shared memory.

Satoh appears to teach a first and second processor (Fig. 32, items 11-1 and 11-2) that access a common synchronous dynamic random access memory (SDRAM) (Fig. 32, item 22). The SDRAM receives a single clock signal (Fig. 32, item CLK). The first and second processors each contain an **independent** clock driver (Fig. 32, item 16 in each of the first and second processors 11-1 and 11-2). One processor may release data, address and clock

lines to the SDRAM from the other processor by controlling the data, address and clock lines to a high impedance state (Satoh, col. 15, lines 60-67).

Satoh's first and second processors each containing an **independent** clock driver is **NOT** a first agent providing a memory access clock signal and a second agent providing **a representation of the memory access clock signal** to access a shared memory **in synchronism with access by the first agent** to the shared memory, as claimed by claims 13 and 16.

Applicant claims an inter-dependence between the clock signals produced between the first and second agents. Claims 13 and 16 recite the second agent's clock signal is a **representation** of a first agent's clock signal. Satoh's agents each contain their own clock signal generator, each **independent** of one another.

Satoh fails to teach the first and second agents (Satoh, items 11-1 and 11-2) are in synchronism. Each of the processing agents in Satoh contain **independent** clock generators (Satoh, items 16 in each of the processing agents). Independent clock generators are by definition not in synchronism.

Accordingly, for at least all the above reasons, claims 13 and 16 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-8, 10-12 and 20-23 over Wu

In the Office Action, claims 1-8, 10-12 and 20-23 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu, U.S. Patent No. 5,659,715 ("Wu"). The Applicants respectfully traverse the rejection.

Claims 1-6 and 20-23 recite, *inter alia*, a second agent having a clock signal representation of a first agent's clock signal. Claims 7-8 and 10-12 recite, *inter alia*, a plurality of agents have clock signal representations of a base clock signal.

Wu appears to teach a first and second processor having access to a common memory bank (Fig. 3, items 302, 400 and 304 respectively). Address

and data lines (Wu, items 306 and 308) running to the common memory bank (Wu, item 304) are routed through a single source, the graphics controller (Wu, item 400). The CPU (item 302) and the graphics controller are tied together to route data to the common memory (Wu, Fig. 3). The common memory is connected with to the graphics controller which is connected to the CPU (WU, Fig. 3) Thus, the CPU, the graphics controller and the common memory are synchronized to pass data and address information therebetween with a common clock signal.

Wu's memory bank synchronizing with the CPU and graphics controller is **NOT** a second agent having a clock signal representation of a first agent's clock signal, as claimed by claims 1-6 and 20-23.

Wu's memory bank synchronizing with the CPU and graphics controller is **NOT** a plurality of agents have clock signal representations of a base clock signal, as claimed by claims 7-8 and 10-12.

Unlike claims 1-8, 10-12 and 20-23, Wu's second agent has a clock signal that is **identical** to the first agent's clock signal. All of the data and address lines are routed through the graphics controller before reaching the common memory, thus making all the components in synchronism with each other to a common clock frequency.

Accordingly, for at least all the above reasons, claims 1-8, 10-12 and 20-23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 14-15 and 17-18 over Satoh in view of Hughes

In the Office Action, claims 14-15 and 17-18 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Satoh in view of Hughes, U.S. Patent No. 5,6784,582 ("Hughes"). The Applicants respectfully traverse the rejection.

Claims 14-15 are dependent on claim 13 and are patentable for the same reasons claim 13 is patentable.

Claims 14-15 recite, *inter alia*, a first agent providing a memory access clock signal and a second agent providing **a representation of the memory access clock signal** to access a shared memory **in synchronism with access by the first agent** to the shared memory. Claims 17-18 recite, *inter alia*, secondly accessing a shared memory from a second agent based on a **representation of a memory access clock signal**.

As discussed above, Satoh fails to teach *both* a first agent providing a memory access clock signal and a second agent providing **a representation of the memory access clock signal** to access a shared memory *and* **synchronism** between a first agent and a second agent to the shared memory.

Hughes appears to disclose an arbiter for controlling access to a shared synchronous memory by a processor complex, a refresh unit, an internal bus, and a core bus (See Hughes, col. 4, lines 1-29; Figure 2).

Hughes' processor complex provides a memory clock signal in addition to memory access request information (See Hughes, col. 4, lines 49-58). This memory clock signal is the only clock signal provided to shared memory (See Hughes, col. 4, lines 55-58; Figure 2). Other users of the shared memory (the refresh unit, internal bus, and core bus) provide only memory access request information, i.e., starting address, size, and a direction (See Hughes, col. 5, lines 35-45). The other users of the shared memory do **not** provide any clock signal to shared memory (See Hughes, Figures 2 and 3).

Hughes discloses a shared memory which is driven by a **single clock signal** from a processor complex. The other users of the shared memory do **not** provide any clock signal, much less **provide a representation** of a memory access clock signal. Thus, Hughes fails to disclose, teach, or suggest a second agent to **provide a representation** of a memory access clock signal to access a shared memory in **synchronism** with access by a first agent, as claimed by claims 14-15 and 17-18.

Thus, even if the combination of Satoh and Hughes where obvious (which it is not), the combination would fail to teach or suggest all of the claimed limitations of claims 14-15 and 17-18.

Accordingly, for at least all the above reasons, claims 14-15 and 17-18 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claim 19 over Satoh in view of Hughes, and further in view of Clayton, IV

In the Office Action, claim 19 was rejected under 35 U.S.C. §103(a) as allegedly being obvious over Satoh in view of Hughes, and further in view of Clayton, IV, U.S. Patent No. 4,476,527 ("Clayton"). The Applicants respectfully traverse the rejection.

Claim 19 is dependent on claim 17 and is patentable for the same reasons claim 17 is patentable.

Claims 19 recites, *inter alia*, secondly accessing a shared memory from a second agent based on a **representation of a memory access clock signal**.

As discussed above, Satoh and Hughes fail to teach secondly accessing a shared memory from a second agent based on a **representation of a memory access clock signal**.

Clayton appears to teach a method of synchronizing the transfer of information over a data bus through the use of a master clock signal. A master clock signal is distributed to peripheral controllers of the data bus through a **single clock line** (Clayton, Abstract). All information transfers are synchronous with the single frequency bus clock, but the data transfers rate is variable and automatically determined by the sending and receiving units (Clayton, Abstract).

Clayton uses only a **single clock line**. A single clock line supplying all of the components supplies the same clock frequency. A same clock frequency is **NOT** a **representation of a memory access clock signal**, as claimed by claim 19.

Thus, even if the combination of Satoh, Hughes and Clayton where obvious (which it is not), the combination would fail to teach or suggest all of the claimed limitations of claim 19.

Accordingly, for at least all the above reasons, claim 19 is patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-8, and 10-23 are patentable over the prior art of record.

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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